Amendments to the Claims:

Claims 1, 11 and 20 have been amended herein. Claims 15 and 16 have been cancelled. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A video conferencing circuit for use with a plurality of video input devices and a video output device, said video conferencing circuit comprising:
video input means configured to select an input video signal from one of a plurality of video signal generating devices, said video input means including a video decoder circuit to receive selected video signals and convert said selected video signals to an input video signal;
a remote interface circuit;
a video output device; and
an application specific integrated circuit (ASIC) connected to said video input means, to said video output device and to said remote interface circuit, said ASIC having:
a high speed serial video input,
a video-in circuit connected to said video input means to receive one of said input video signal from one of said plurality of video signal generating devices and said high speed serial video input, said video-in circuit including an input configuration circuit connected to receive one of a plurality of video input signals and a high speed serial video input, a control register connected to said video processing means to receive control signals therefrom and said input configuration circuit to supply input control signals to cause said input configuration circuit to operate to supply said one of said plurality of video input signals as said input video signal to said memory circuit,
a memory circuit connected to said video-in circuit to receive said one of said input video signal and said high speed serial video input, said memory circuit being

configured to retain and transmit said one of said input video signal and said high speed serial video input as stored data,

data compression means connected to said memory circuit to receive said stored data and to compress said stored data through an encoding process to form outgoing compressed data,

video processing means connected to receive said outgoing compressed data and connected to said remote interface circuit to transmit said outgoing compressed data and to receive incoming compressed data from a remote station, said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween,

video decompression means connected to said video processing means to receive said incoming compressed data and configured to decompress and to transmit said incoming compressed data to said memory circuit, said memory circuit being configured to convert said incoming compressed data to incoming stored data, and

video image out means connected to receive incoming stored data from said memory circuit and to transmit said incoming stored data as a video image signal to a video display device;

wherein said memory circuit includes a memory structure and a memory control circuit to convert said one of said input video signal and said high speed serial video input to stored data and to convert said incoming compressed data to incoming stored data and wherein said output of said input configuration circuit is supplied to a decimation circuit which operates to reduce the density of the said output signal and is connected to a buffer to store and transmit an output which is a video.

2. (original) The video conferencing circuit of claim 1 wherein said remote interface circuit includes a modem.

3. (Cancelled)

4. (previously presented) The video conferencing circuit of claim 1 wherein said memory structure is a DRAM configured to receive and store said stored data and said incoming stored data.

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (original) The video conferencing circuit of claim 1 further including a data bus interconnected between said video-in circuit, said memory circuit, said encoding circuit, said decoding circuit and said video out circuit for transmitting control signals therebetween, and wherein said video processing means includes a bus control circuit connected to said data bus to supply said control signals thereto.

9. (previously presented) The video conferencing circuit of claim 8 wherein said bus control circuit includes a backbone interface circuit connected to said data bus, said backbone interface circuit being configured to generate and to supply said control signals to said data bus.

10. (previously presented) The video conferencing circuit of claim 9 wherein said video processing means includes a data processor connected to said remote interface circuit, a processor interface connected to said data processor to supply data thereto and a arbitration and control circuit connected to said processor interface and to said backbone interface circuit and configured to select and activate one of the backbone interface circuit and the processor interface, and a host interface circuit connected to said arbitration and control circuit, said host interface circuit being configured to supply to and receive data from the processor interface and the backbone interface circuit, said arbitration and control circuit also being connected to supply and receive video signals to and from an external device for obtaining and displaying video images.

11. (currently amended) A video conferencing circuit for use with a plurality of video output devices and a video input device, said video conferencing circuit comprising:

video output means configured to select one of a plurality of video output devices to receive an output video signal;

a remote interface circuit;

a video input device; and

an application specific integrated circuit (ASIC) connected to said video input device, to said video output means and to said remote interface circuit, said ASIC having:

a high speed serial video input,

a video-in circuit connected to said video input device to receive one of a video input signal from said video input device and ~~a~~ said high speed serial video input,

a memory circuit connected to said video-in circuit to receive said one of said video input signal and said high speed serial video input, said memory circuit being configured to retain and transmit said one of said video input signal and said high speed serial video input as stored data,

data compression means connected to said memory circuit to receive said stored data and to compress said stored data through an encoding process to form outgoing compressed data,

video processing means connected to receive said outgoing compressed data and connected to said remote interface circuit to transmit said outgoing compressed data and to receive incoming compressed data from a remote station, ~~said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween~~,

video decompression means connected to said video processing means to receive said incoming compressed data and configured to decompress and to transmit said incoming compressed data to said memory circuit, said memory circuit being configured to convert said incoming compressed data to incoming stored data, said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween, and

video image out circuit connected to receive incoming stored data from said memory circuit and to transmit said incoming stored data as a video image signal to said one of said plurality of video output devices of said video output means;

wherein said memory circuit includes a memory structure and a memory control circuit to convert said one of said video input signals and said high speed serial video input to stored data and to convert said incoming compressed data to incoming stored data;

wherein said video-in circuit includes an input configuration circuit connected to receive said video input signal and said high speed serial video input, a control register connected to said video processing means to receive control signals therefrom and said input configuration circuit to supply input control signals to cause said input configuration circuit to operate to supply said one of said video input signal and said high speed serial video input to said memory circuit; and

wherein said output of said input configuration circuit is supplied to a decimation circuit which operates to reduce the density of the said output signal and is connected to a buffer to store and transmit an output which is a video .

12. (original) The video conferencing circuit of claim 11 wherein said remote interface circuit includes a modem.

13. (cancelled)

14. (previously presented) The video conferencing circuit of claim 11 wherein said memory structure is a DRAM configured to receive and store said stored data and said incoming stored data.

15. (cancelled)

16. (cancelled)

17. (previously presented) The video conferencing circuit of claim 11 further including a data bus interconnected between said video–in circuit, said memory circuit, said encoding circuit, said decoding circuit and said video out circuit for transmitting control signals therebetween, and wherein said video processing means includes a bus control circuit connected to said data bus to supply said control signals thereto.

18. (previously presented) The video conferencing circuit of claim 17 wherein said bus control circuit includes a backbone interface circuit connected to said data bus, said backbone interface circuit being configured to generate and to supply said control signals to said data bus.

19. (previously presented) The video conferencing circuit of claim 18 wherein said video processing means includes a data processor connected to said remote interface circuit, a processor interface connected to said data processor to supply data thereto and a arbitration and control circuit connected to said processor interface and to said backbone interface circuit and configured to select and activate one of the backbone interface circuit and the processor interface, and a host interface circuit connected to said arbitration and control circuit, said host interface circuit being configured to supply to and receive data from the processor interface and the backbone interface circuit.

20. (currently amended) A video conferencing circuit for use with a plurality of video output devices and a video input device, said video conferencing circuit comprising:

video output means configured to select one of a plurality of video output devices to receive an output video signal;

a remote interface circuit;

a video input device; and

an application specific integrated circuit (ASIC) connected to said video input device, to said video output means and to said remote interface circuit, said ASIC having:

a high speed serial video input,

a video-in circuit connected to said video input device to receive one of a video input signal from said video input device and said high speed serial video input,

a memory circuit connected to said video-in circuit to receive said one of said video input signal and said high speed serial video input, said memory circuit being configured to retain and transmit said one of said video input signal and said high speed serial video input as stored data,

data compression means connected to said memory circuit to receive said stored data and to compress said stored data through an encoding process to form outgoing compressed data,

video processing means connected to receive said outgoing compressed data and connected to said remote interface circuit to transmit said outgoing compressed

data and to receive incoming compressed data from a remote station, ,

video decompression means connected to said video processing means to receive said incoming compressed data and configured to decompress and to transmit said incoming compressed data to said memory circuit, said memory circuit being configured to convert said incoming compressed data to incoming stored data, said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween,

video image out circuit connected to receive incoming stored data from said memory circuit and to transmit said income to transmit said incoming stored data as a video image signal to said one of said plurality of video output devices of said video output means;

~~The video conferencing circuit of claim 11 wherein said video image out circuit includes~~:

a memory control sequencer connected to said memory circuit, said memory control sequencer being configured to generate and send to the memory circuit instructions to cause the supply said memory circuit to supply said memory control sequencer with said incoming stored data and said memory control sequencer being configured to supply said incoming stored data as an output,

a line buffer connected to receive said incoming stored data from said memory control sequencer, said line buffer being configured to store a video line of said incoming stored data as first video out signal and another video line of said stored video data as a second video out signal,

an interpolator circuit connected to said line buffer to receive said first video out signal and said second video out signal and to generate an interpolated video signal,

a buffer connected to said interpolator circuit to receive said interpolated video signal therefrom,

a control register connected to said data bus to receive control signals from said video processing control and to said buffer to supply signals to cause said buffer to supply said interpolated video ~~signal ,~~ signal, and

an encoder connected to said buffer to receive said interpolated video signal therefrom and to said control register to receive signals to cause said interpolated video signal to be supplied as the video image signal to one of said plurality of video output devices of said video output means;

wherein said memory circuit includes a memory structure and a memory control circuit to convert said one of said video input signals and said high speed serial video input to stored data and to convert said incoming compressed data to incoming stored data.

21. (canceled)

22. (cancelled)

23. (cancelled)

24. (cancelled)